

Atty Docket No. JCLA10688-R

Serial No.: 10/604,128

REMARKS**Present Status of the Application**

The Office Action rejected Claims 1-13 under 35 USC 102(b) as being anticipated by Morita (US 2002/0190974 A1, hereinafter "Morita").

After traversing of the aforementioned rejections and amending the claims, Claims 1-13 remain pending in the present application.

Discussion of the claim rejection under 35 USC 102

The Office Action has rejected Claims 1-13 under 35 U.S.C. 102(b) as being anticipated by Morita (US-2002/0190974A1, hereinafter "Morita").

Applicants respectfully traverse the above rejections as set forth below.

Amended Claims 1 and 6 of the present invention includes the following added claim limitation: "the driving circuit does not include a digital to analog converter (DAC)".

As was previously acknowledged by the Examiner in the previous telephone interview with Applicant's representative, the above claim limitation of "the driving circuit does not include a digital to analog converter (DAC)" is clearly not taught by Morita.

Furthermore, the inverter 182₀₋₁ found in FIG. 26 in Morita, as cited by the Examiner in the Office Action, for VG₀₋₁ is not used for the same element and not used for the same function as the inverter in Claim 1 of the present invention and is clearly not applicable for rejection under

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anticipation. Therefore, the inverter in Morita is not equivalent to the “inverter” claimed in Claim 1 of the present invention, thus no anticipation is found.

The inverter 182₀₋₁ found in FIG. 26 in Morita is used as a part of the VG₀₋₁, which is found in FIG. 16 in Morita as part of the signal line drive circuit 40₀. On the other hand, the inverter 206 in the present invention is used by itself to accomplish the similar purpose as the DAC shown in FIGs 13A, 13B, and 13C in Morita but at much less power consumption and NOT of the same purpose as the signal line drive circuit 400. As described in paragraphs [0006] & [0025] of the present invention: “...uses the inverter to output the color output signal to the displayAs the invention does not require use of digital to analog converter, which consume a large amount of power, it can achieve the object of saving power.” and “... replaces the digital to analog converter 108 with the inverter.” On the other hand, Morita clearly uses the digital analog converter instead of an inverter as described in FIG. 2 (DAC 38), FIGs 13A, 13B, 13C (DAC 38_A 38_B 38_C), and FIG. 16 (DAC₀₋₁ - DAC₀₋₂₄) in Morita.

For reason discussed above, Claims 1 and 6 are patentably distinguished over Morita, and should be allowed.

Dependent Claims 2-5 and Claims 7-13 are allowable for at least the same reasons discussed above in connection with Claims 1 and 6.

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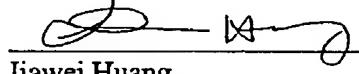
CONCLUSION

For at least the foregoing reasons, it is believed that all the pending Claims 1-13 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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